Computer Architecture and Organisation :

Computer Architecture → It is concerned with structure and behavior of computer as seen by user. It include information format, instruct set & techniques for addressing memory.

Computer Organization → It is concerned with the way h/w components operate & the way they are connected together to form the computer system.

Basic computer data type → Number, Conversion (B D H O)

Complements → 1's 2's 9's 10's

Fixed point Representation

(There is fixed no. of digits after decimal part)

word size → bit

- Integer
  - Unsigned
    - 8 bit 0-255
    - 16 bit 0-65535
    - 0 to +ve
  - Signed
    - Signed Magnitude
    - 1's complement
    - 2's complement
- Fraction

→ When integer binary no. is +ve, the sign is represented by 0 and magnitude by a +ve binary number.

→ When no. is negative, the sign is represented by 1 but rest of no. may be represented in one of 3 possible ways.

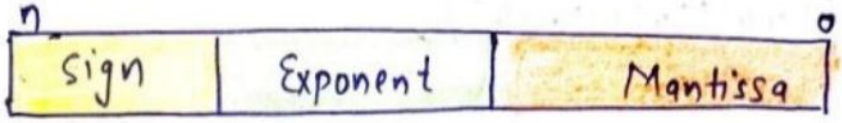
Floating point Representation ⇒ It has two part:

→ The first part represents a signed fixed point no. called **mantissa**. Mantissa may be fraction or integer.

→ The second part of designates the position of decimal point & is called **exponent**.

→ Floating point is always interpreted to represent a no. in the following form: $m \times r^e$

→ mantissa ⇒ m & exponent e are physically represented in register. The radix r & the radix point position of mantissa.



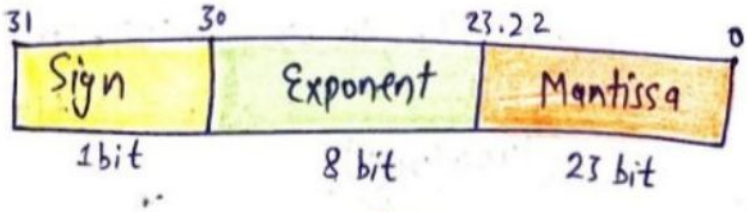
+7.32

It has 3 parts :— Mantissa, Base, Exponent

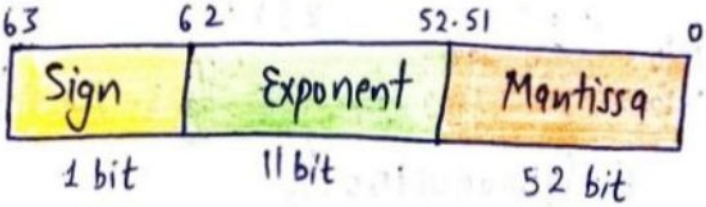
Number	Mantissa	Base	Exponent
5×10^2	5	10	2
212.22	21222	10	-2
55×2^6	55	2	6

IEEE 754 Floating point number representation :—

(a) **Single precision format**: 32 bit



(b) **Double precision format**: 64 bit



Examples of fixed point Number Representation

Eg-1 Compute 0.75 + (−7.5) using fixed point Numbers.

Ans-

Step-① 0.75

$(0000.1100)_2$

0.75 × 2 = 1.5
0.5 × 2 = 1.0
0.0 × 2 = 0.0
⋮
0.0

Step-② −7.5

0111.1000

2's compl. $(1000.1000)_2$

0.5 × 2 = 1.0
0.0 × 2 = 0.0

00001100
10001000
10001100

$(-6.75) \Leftarrow (1001.0100)_2$ ✓

Eg-2 Assume −43.625 convert into binary with 1 bit for sign, 15 bits for integer & 16 bits for fraction.

2	43	→
2	21	1
2	10	1
2	5	0
2	2	1
	1	0

101011

0.625 × 2 = 1.25
0.25 × 2 = 0.50
0.50 × 2 = 1.0
0.0 × 2 = 0.0
10100---

1000000000101011.1010000000000000

Register Transfer Language ⇒ It is the symbolic representation of notations used to specify the sequence of micro-operations.

→ Information transfer from one register to another register is called Register Transfer.

→ Registers are designated by capital letters, sometimes followed by numbers (eg- A, R1, R13, IR)

$$\left[\begin{array}{l} \text{No. of Mux} = \text{No. of bits in Register} \\ \text{No. of I/p. in Mux (sizeof)} = \text{No. of Register} \end{array}\right]$$

Q: A common bus system for 16 registers of 32 bits each.

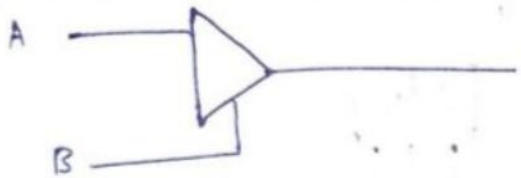
(i) Selection inputs = $2^4 = 2^n \Rightarrow \boxed{n=4}$

(ii) 16 X 1

(iii) 32 multiplexer

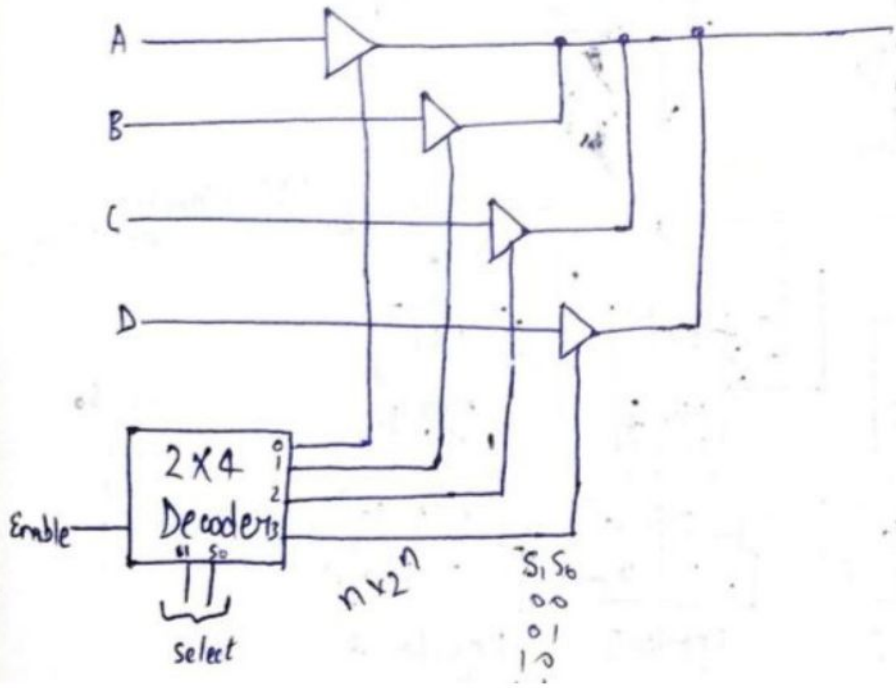
Tri-state Gates :- It is a digital circuit that has 3 gates two of which are signals equivalent to logic 1 & 0 as in a conventional gate. However, the third gate exhibits a high-impedance gate.

→ The most commonly used 3 state gates in case of bus system is a buffer gate.



Y = A if C = 1
High impedance if C = 0

Bus line with 3 state Buffer:-



One line Common Bus system using Three state Gate Buffer

is called multiple pass assembler.
Here assembler divide these tasks in 2 passes

Pass 1 :- Define symbols & literals and remember them in symbol table & literal table respectively.
keep track of location counter.
Process pseudo-operation

Pass 2 :- Generate object code by converting symbolic op-code into respective numeric op-code.
Generate data for literals and look for values of symbols.

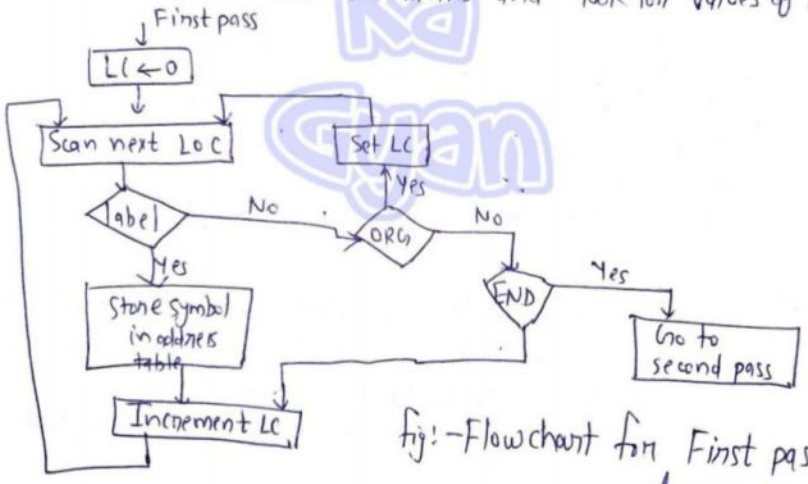


fig:- Flowchart for First pass of assembler

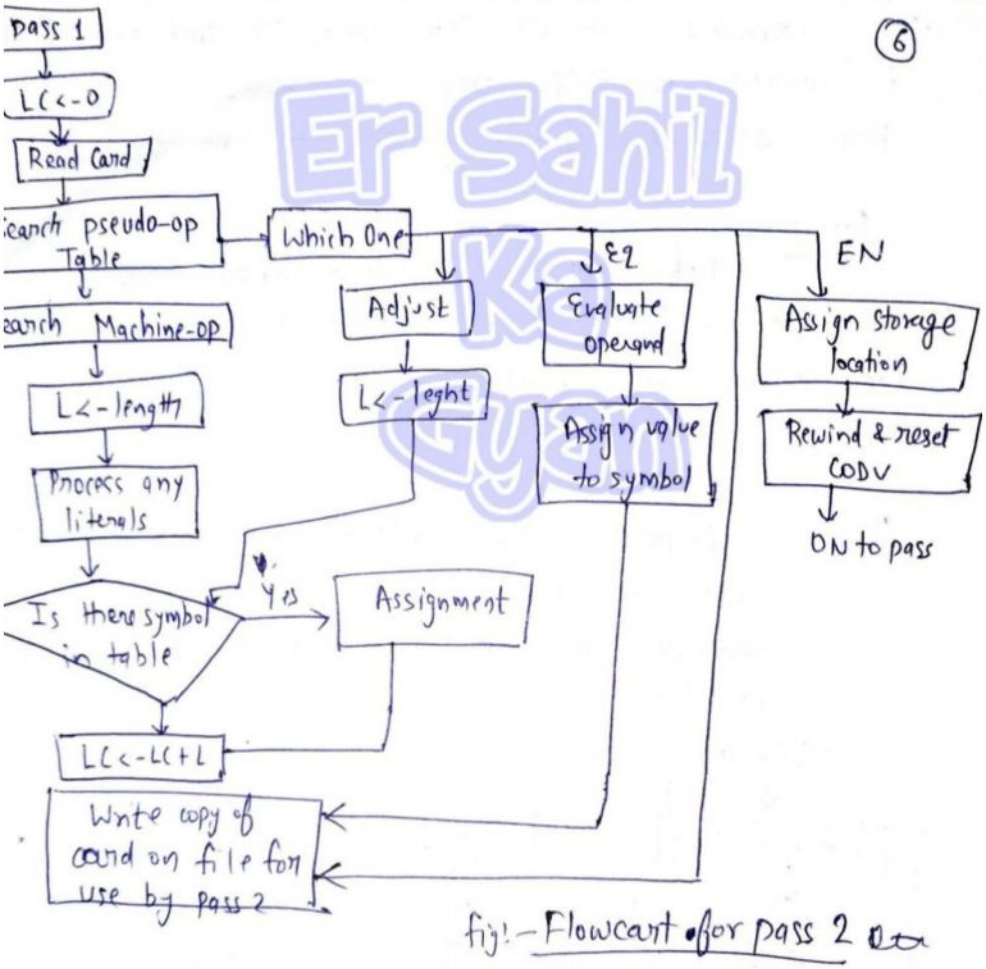


fig:- Flowcart for pass 2

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